**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 208

**ISSUE TITLE:** Clock-Data Pin Relationship Keyword

**REQUESTOR:**  Michael Mirmak, Intel Corp.

**DATE SUBMITTED:** October 6, 2020

**DATE REVISED:**

**DATE ACCEPTED:** January 8, 2021

**DEFINITION OF THE ISSUE:**

IBIS supports descriptions of individual models, their behavior, and evalution of their performance. IBIS also supports descriptions of component pins and interconnects between pins and models. However, IBIS lacks descriptions of architectural relationships between models as assigned to pins, particularly where those relationships must be included in system signal integrity simulations. The relationship of most interest at the time of writing is that between data signals and clock inputs.

This BIRD defines a new keyword, [Clock Pins], which makes explicit which pins on a component are used for supplying clock information relative to data, whether input or output, or another clock.

Modification to [Algorithmic Model] may be needed in order to define an architecture that includes both data I/O and an additional input connection for the clock.

Note that this solution does not address the more difficult case, where instances of clocked data buffers require clock connections entirely internal to the same [Component] as the data buffers.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. IBIS must support defined links between clock signals and data buffers in clocked architectures where the clock signal is supplied external to the [Component] | This is different than BIRD 207, where parameters are defined to support the AMI model being informed of the signal and component with which it is associated; this BIRD informs the EDA tool of the association.  Similarly, BIRD 204 specifies the kind of clock data to be supplied to a given clock-forwarded AMI model, but not the specific timing relationship between clock and data. |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table : IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| [Clock Pins] | New | A new keyword is added, hierarchically under [Component] |

**PROPOSED CHANGES:**

The following keyword shall appear immediately after [Diff Pin] in the specification.

*Keyword:* **[Clock Pins]**

*Required:* No

*Description:* This optional keyword identifies clocking relationships between pins for a specific [Component] keyword.

Sub-Params: clocked\_pins, relationship

*Usage Rules:* The keyword arguments consist of three columns of entries, beginning on the same line as the keyword itself. The keyword [Clock Pins] shall be followed by the string “clocked\_pins” and “relationship”, all separated by whitespace. The second and any following lines consist of two columns of pin names and a string column as detailed below.

Column 1 is required and lists clock pins, one clock pin per line. These are pins from the [Pin] keyword pin\_name column that correspond to clocks, either inputs or outputs, for the component.

Column 2 is required and lists clocked pins. These are the pins from the [Pin] keyword pin\_name column that correspond to clocked data pins for the component. The pin named in the second column of each line is assumed to be “clocked” by the pin named in the first column.

Alternatively, column 2 may contain the pin\_name of a clock pin where a timing relationship (for example, a timing skew) exists with respect to the clock pin\_name in column 1. The pins listed in columns 1 and 2 are assumed to be Inputs, Outputs, I/Os, 3-state, or Open variants of these Model\_types. Included in these are the “\_ECL” and “\_diff” variants.

Column 3 is required and contains a string identifying the timing relationship between the pins listed in columns 1 and 2. The only permitted entry is “Unspecified”, which is case-sensitive. This column is intended for future expansion.

Three entries, separated by whitespace, are required per line.

Entire lines may not be duplicated. The same pin\_name may not appear in both columns of any single line.

[Clock Pins] is compatible with [Diff Pin], in that the clock pins and data pins may be single-ended or differential. For differential pins, the [Clock Pins] line shall list only the non-inverting pin(s) of the differential pair(s) as listed under the first column of the [Diff Pin] keyword.

Some Model\_types are incompatible with the [Clock Pins] keyword. For both columns, prohibited Model\_types include Series, Series\_switch, and Terminator. Pins associated with [Model]s of these types shall not appear under [Clock Pins]. [Clock Pins] is not compatible with pin\_names in [Series Pin Mapping] or function\_table\_group states in [Series Switch Groups].

*Other Notes:* [Clock Pins] is hierarchically under the [Component] keyword.

The structure of [Clock Pins] assumes that the clocking relationships cannot be redefined dynamically for the given [Component] (for example, the number of data pins supported by any one clock pin is fixed).

[Clock Pins] is compatible with [Algorithmic Model], [External Model], [External Circuit] and their associated keywords. [Clock Pins] is also compatible with [Model Selector].

[Clock Pins] is also compatible with the [Component] keyword Timing\_location subparameter.

*Example:*

[Clock Pins] clocked\_pins relationship

A1 B1 Unspecified | Data pin B1 uses clock information from Pin A1

A2 B2 Unspecified | Data pin B2 uses clock information from Pin A2

A3 B3 Unspecified

A3 B4 Unspecified | Pins B3, B4, B5 use clock information from A3

A3 B5 Unspecified | case-sensitive entry

**BACKGROUND INFORMATION/HISTORY:**

Note that the solution requires a keyword within the [Component] keyword but not within [Model], as the clock-data connection is between \*instances\* of clock and data models, not between the model structures themselves. [Model] and [Algorithmic Model] define the behavior of a design type. Only the [Pin] list instantiates individual [Model]s. In other words, in an interface with multiple data pins with identical buffer behaviors defined by a single [Model], the interface data pin buffers are not clocked by another [Model] defining clock behaviors; instead, each of the data pin buffers is associated with clocking from another \*pin\*, which corresponds to an \*instance\* of a clock [Model].

This BIRD can co-exist easily with, but is not dependent on, BIRD204 which defines the kind of clock input data the AMI model can accept. Similarly, this BIRD supplements the clock forwarding functions of BIRD207, but by notifying the EDA tool of timing relationships rather than notifying the AMI model of component and signal associations.

A future BIRD may be written to create a related keyword for defining additional timing relationships as named in the third column here or named elsewhere. The third column information may also be expanded in a later BIRD to support filenames, where the named file contains the timing relationship definition.

This BIRD was reviewed, and significant alterations provided, by Eric Brock and Walter Katz of MathWorks, Bob Ross of Teraspeed Labs, and Curtis Clark of ANSYS.

The BIRD was reviewed with discussion several times in September and October 2020 in the IBIS-ATM Task Group meeting and approved by them without objection for submission as a BIRD on October 6, 2020.