**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 191.2

**ISSUE TITLE:** Clarifying Locations for Si\_location and Timing\_location

**REQUESTOR:**  Bob Ross, Teraspeed Labs

**DATE SUBMITTED:** June 28, 2017

**DATE REVISED:** August 04, 2017; August 08, 2017

**DATE ACCEPTED:** September 15, 2017

**DEFINITION OF THE ISSUE:**

The Interconnect Modeling BIRD189 defines three separate interfaces as Buffer and Pad (for die pad) and Pin. The [Component] subparameters for Si\_location and Timing\_location only provide Die and Pin options. Originally BIRD191 introduced a new “Buffer” option. However, BIRD191.1 is changed to just clarify that when there is a choice between a buffer location and a die location due to how an Interconnect Model Set may be configured, the location “Die” always means the buffer location. This makes the “Die” location consistent with the existing package model options and when an [Interconnect Model Set] is used. Some arguments for this interpretation are given at the end.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Clarify what the “Die” selection for Si\_location and Timing\_location means when Buffer and Pad (die pad) locations are both available
 | The Interconnect Modeling BIRD189.x divides the existing “Die” location (which can mean buffer) into Buffer and Pad (which can mean die pad) |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table : IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| Under [Component], Si\_location and Timing\_location add clarification ofr the “Die” selection  | Text |  |

**PROPOSED CHANGES:**

*On page 20 under the [Component] keyword, replace:*

*Keyword:* [Component]

*Required:*        Yes

*Description:* Marks the beginning of the IBIS description of the integrated circuit named after the keyword.

*Sub-Params:*   Si\_location, Timing\_location

*Usage Rules:*   If the .ibs file contains data for more than one component, each section must begin with a new [Component] keyword.  The length of the component name must not exceed 40 characters, and blank characters are allowed.

NOTE: Blank characters are not recommended due to usability issues.

Si\_location and Timing\_location are optional and specify where the Signal Integrity and Timing measurements are made for the component.  Allowed values for either subparameter are “Die” or “Pin”.  The default location is at the “Pin”.

*Example:*

[Component]     7403398 MC452

|

Si\_location     Pin    | Optional subparameters to give measurement

Timing\_location Die    | location positions

With (proposed change in red):

*Keyword:* [Component]

*Required:*        Yes

*Description:* Marks the beginning of the IBIS description of the integrated circuit named after the keyword.

*Sub-Params:*   Si\_location, Timing\_location

*Usage Rules:*   If the .ibs file contains data for more than one component, each section must begin with a new [Component] keyword.  The length of the component name must not exceed 40 characters, and blank characters are allowed.

NOTE: Blank characters are not recommended due to usability issues.

Si\_location and Timing\_location are optional and specify where the Signal Integrity and Timing measurements are made for the component.  Allowed values for either subparameter are “Die” or “Pin”. For pins that connect to a buffer through an [Interconnect Model Set], keyword described below, the “Die” selection shall be at the buffer terminal location. The default location is at the “Pin”.

*Example:*

[Component]     7403398 MC452

|

Si\_location     Pin    | Optional subparameters to give measurement

Timing\_location Die    | location positions

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On page 104 in IBIS Version 6.1, change at-pad to at-buffer terminal (shown in red)

From:

IMPORTANT: measurements for receivers in IBIS are normally assumed to be conducted at the die pads/pins. In such cases, the electrical input model data comprises a “load” which affects the waveform seen at the pads. However, for models measure the analog input response at the die pads or inside the circuit (this does not preclude tools from reporting digital D\_receive and/or analog port responses in addition to at-pad A\_signal response). If at-pad measurements are desired, the A\_signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter then effectively acts “in parallel” with the load of the circuit. If internal measurements are desired (e.g., if the user wishes to view the signal after processing by the receiver), the user-defined signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter is effectively “in series” with the receiver model. The vhigh and vlow parameters should be adjusted as appropriate to the measurement point of interest.

To:

IMPORTANT: measurements for receivers in IBIS are normally assumed to be conducted at the die pads/pins. In such cases, the electrical input model data comprises a “load” which affects the waveform seen at the pads. However, for models measure the analog input response at the die pads or inside the circuit (this does not preclude tools from reporting digital D\_receive and/or analog port responses in addition to at-buffer terminal A\_signal response). If at-buffer terminal measurements are desired, the A\_signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter then effectively acts “in parallel” with the load of the circuit. If internal measurements are desired (e.g., if the user wishes to view the signal after processing by the receiver), the user-defined signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter is effectively “in series” with the receiver model. The vhigh and vlow parameters should be adjusted as appropriate to the measurement point of interest. In this case, both A\_signal port and user-defined signal ports shall be listed in the Ports subparameter.

On page 110 of IBIS Version 6.1, change at-pad to at-buffer terminal: (shown in red)

From:

If at-pad or at-pin measurement using a SPICE, IBIS-ISS, Verilog-A(MS) or VHDL-A(MS) [External Model] is desired, the vlow and vhigh entries under the A\_to\_D subparameter must be consistent with the values of the [Diff Pin] vdiff subparameter entry (the vlow value must match -vdiff, and the vhigh value must match +vdiff). The logic states produced by the A\_to\_D conversion follow the same rules as for single-ended buffers, listed above. An example is shown at the end of this section.

IMPORTANT: For true-differential buffers under [External Model], the user can choose whether to measure the analog input response at the die pads or internal to the circuit (this does not preclude tools from reporting digital D\_receive and/or analog responses in addition to at-pad A\_signal response). If at-pad measurements for a SPICE, IBIS-ISS, Verilog-A(MS) or VHDL-A(MS) model are desired, the A\_signal\_pos port would be named in the A\_to\_D line under port1 and A\_signal\_neg under port2. The A\_to\_D converter then effectively acts “in parallel” with the load of the buffer circuit. If internal measurements are desired (e.g., if the user wishes to view the signal after processing by the input buffer), the user-defined analog signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter is “in series” with the receiver buffer model. The vhigh and vlow parameters should be adjusted appropriate to the measurement point of interest, so long as they as they are consistent with the [Diff Pin] vdiff declarations.

To:

If at-buffer terminal or at-pin measurement using a SPICE, IBIS-ISS, Verilog-A(MS) or VHDL-A(MS) [External Model] is desired, the vlow and vhigh entries under the A\_to\_D subparameter must be consistent with the values of the [Diff Pin] vdiff subparameter entry (the vlow value must match -vdiff, and the vhigh value must match +vdiff). The logic states produced by the A\_to\_D conversion follow the same rules as for single-ended buffers, listed above. An example is shown at the end of this section.

IMPORTANT: For true-differential buffers under [External Model], the user can choose whether to measure the analog input response at the die pads or internal to the circuit (this does not preclude tools from reporting digital D\_receive and/or analog responses in addition to at-buffer terminal A\_signal response). If at-buffer terminal measurements for a SPICE, IBIS-ISS, Verilog-A(MS) or VHDL-A(MS) model are desired, the A\_signal\_pos port would be named in the A\_to\_D line under port1 and A\_signal\_neg under port2. The A\_to\_D converter then effectively acts “in parallel” with the load of the buffer circuit. If internal measurements are desired (e.g., if the user wishes to view the signal after processing by the input buffer), the user-defined analog signal port would be named in the A\_to\_D line under port1. The A\_to\_D converter is “in series” with the receiver buffer model. The vhigh and vlow parameters should be adjusted appropriate to the measurement point of interest, so long as they as they are consistent with the [Diff Pin] vdiff declarations. In this case, A\_signal\_pos and A\_signal\_neg ports and user-defined signal ports shall be listed in the Ports subparameter.

**BACKGROUND INFORMATION/HISTORY:**

BIRD191 is needed to overcome a technical omission in BIRD189.x. BIRD191 should appear in the same release as BIRD189.x. This could be regarded as a quick, but necessary fix.

Working on BIRD161.x is suggested as an option. However, it contains much material that would not be quickly vetted for approval and adoption in the next release. Moreover, some content has been handled in other BIRDs and other content presupposes some structures that are still in discussion and debate.

Because they are closely connected, this BIRD’s technical change could have been included in BIRD189.x.

BIRD191.1 changes the title and adopts a different rule. “Die” will be the buffer location in all cases for consistency and simplicity:.

1. “Die” is the same location as standard IBIS with just package models so that there is no difference with or without an available [Interconnect Model Set]
2. “Die” is always the same location with [Interconnect Model Set] keywords that documents buffer-to-pad-to-pin,paths or direct buffer-to-pin paths (where pad is not defined)
3. There is no need for different calculations for the same [Model] at different pins because of possible differences in the on-die interconnect structure
4. There is no need for dealing with on-die coupling effects for multiple Buffer\_I/O’s

To avoid terminology confusion for [Model]/[External Model] terminals, “at-pad” is renamed designated as “at-buffer terminal” in five locations. Die pad terminals and buffer terminals are identical

A sentence is added that certain A\_to\_D and D\_to\_A and reserved names shall be listed in Ports.

This BIRD does not propose any syntax or parser change.

BIRD191.2 has some formatting corrections from Michael Mirmak.