**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 164

**ISSUE TITLE:** Allowing Package Models to be defined in [External Circuit]

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**STATEMENT OF THE ISSUE:**

Package modeling constructs in the current IBIS specifications are insufficient and archaic and cannot be used to properly represent today’s packages and technologies. Modern day packages are modeled using 3D electromagnetic tools that may generate either complex multiport S-parameter models or equivalent SPICE models. There is no direct or indirect way to appropriately consume these package models in the current IBIS specification.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

Package models can be integrated in the IBIS environment using the [External Circuit] keyword that now allows IBIS-ISS as one of its supported languages. When such a model is referenced in the [External Circuit], a sub-parameter will indicate that the subcircuit referenced in the [External Circuit] describes a package model, and will supersede any other definition of the package at other places in the .ibs file. These could include the trace segments under the [Pin Numbers] or RLC matrices under the [Define Package Model] and the [End Package Model] keywords.

**ANY OTHER BACKGROUND INFORMATION:**

In IBIS specification, version 6, Table 11, Page 90, change from

[External Circuit] References enhanced descriptions of structures on the die,

[End External Circuit] including digital and/or analog, active and/or passive circuits

To

[External Circuit] References enhanced descriptions of structures on the die or package

[End External Circuit] including digital and/or analog, active and/or passive circuits

Page 92, add

[External Circuit] may also be used to describe a package model with the sub-parameter Package\_Model described below.

after

In the case of the [External Circuit], however, one can model a circuit having any number of ports

(see definitions below). For example, the ports may include impedance or buffer strength selection

controls in addition to the usual signal and supply connections.

Page 118, change

Sub-Params: Language, Corner, Parameters, Converter\_Parameters, Ports, D\_to\_A, A\_to\_D

To

Sub-Params: Language, Corner, Parameters, Converter\_Parameters, Ports, D\_to\_A, A\_to\_D, Package\_Model

Page 123 add

Package\_Model:

The presence of the subparameter Package\_Model tells the tool that the circuit described in the [External Circuit] is a of a package structure. When present, the package model will supersede any other package model definition for the component and all other package keywords will be over ridden by this [External Circuit].

After

Note that, while the port assignments and SPICE, IBIS-ISS, Verilog-A(MS) or VHDL-A(MS)

model data must be provided by the user, the D\_to\_A and A\_to\_D converters will be provided

automatically by the tool. There is no need for the user to develop external SPICE, IBIS-ISS,

Verilog-A(MS) or VHDL-A(MS) code specifically for these functions.

Page 125, add

Example [External Circuit] describing a package using IBIS-ISS:

[External Circuit] Package-ISS

Package\_Model

Language IBIS-ISS

|

| Corner corner\_name file\_name circuit\_name (.subckt name)

Corner Typ package\_typ.spi package\_typ

Corner Min package \_min.spi package \_min

Corner Max package \_max.spi package \_max

Before

Example [External Circuit] using VHDL-AMS:

Page 129, add

When the [External Circuit] is a Package Model, pin names in the second column of Port\_map refer to the actual pin name (and not implicit pad names), and for the die side of the [External Circuit] the second column of Port\_map refers to explicit pad names (declared by the [Node Declarations] keyword) or [Model] instance terminal names.

Before

Examples:

NOTE REGARDING THIS EXAMPLE: